CLAIMS:

1. A nonvolatile memory array including:

a first plurality of electrically conductive lines (hereinafter "word lines");

a second plurality of electrically conductive lines (hereinafter "bit lines");

a plurality of memory cells, each memory cell being located at an intersection region of one of the word lines and one of the bit lines; and

a read/write circuit for reading/writing a data word including a plurality of bits; the circuit being operative to map each pair of sequential bits of the data word to a respective pair of memory cells located at intersection regions of both a different word line and a different bit line.

2. A nonvolatile memory array as claimed in claim 1, wherein the read/write circuit is operative to write a data word of a plurality of sequential bits b_i ($i = 1...N$) by reading a current value of bit b_i and only performing a writing operation for bit b_i if the current value and a new value of b_i differ; and performing the conditional write operation for bit b_i and the read operation for bit b_{i+1} simultaneously.

3. A nonvolatile memory array as claimed in claim 1, wherein a data word includes a plurality of sequential bits b_i ($i = 1...N$) indicated by a word memory address; the read/write circuit being operative to convert the word memory address to a corresponding physical memory address for bit b_1 which includes a word line number y_1 and a bit line number x_1 and to generate respective bit addresses for the successive bits in the word by each time incrementing the bit line number and changing the word line number ($y_{i+1} \neq y_i$).

4. A nonvolatile memory array as claimed in claim 3, wherein the read/write circuit is operative to determine y_{i+1} as:

$y_{i+1} = y_1 + ((x_1 + i + 1) \text{ MOD } 2)$, if y_1 is odd and

$y_{i+1} = y_1 - ((x_1 + i + 1) \text{ MOD } 2)$, if y_1 is even,

for i=1..N-1

5. A nonvolatile memory array as claimed in claim 1, wherein the read/write circuit is operative to map a group of a plurality of words with respective sequential addresses such that for each word W_i and W_k of the group a sequentially last bit of word W_i and a sequentially first bit of word W_k are mapped to a respective pair of memory cells located at intersection regions of both a different word line and a different bit line.

6. A nonvolatile memory array as claimed in claim 1, wherein each memory cell includes a magnetic tunnel junction.

7. A nonvolatile memory array as claimed in claim 6, wherein each memory cell includes a selection device electrically connected in series with the magnetic tunnel junction.

8. A method of converting an address for accessing a data word in a nonvolatile memory as claimed in claim 1 to a sequence of identifications of memory locations, where a data word includes a plurality of sequential bits b_i ($i = 1...N$) indicated by a word memory address; the method including converting the word memory address to a corresponding physical memory address for bit b_1 which includes a word line number y_1 and a bit line number x_1 and to generate respective bit addresses for the successive bits in the word by changing the bit line number ($x_{i+1} \neq x_i$) and changing the word line number ($y_{i+1} \neq y_i$), for $i = 1 .. N-1$.

9. A method of converting an address as claimed in claim 8, wherein in the step of changing the bit line number includes incrementing the bit line number.

10. A method of converting an address as claimed in claim 9, wherein the step of changing the word line number includes determining y_{i+1} as:

$y_{i+1} = y_1 + ((x_1 + i + 1) \text{ MOD } 2)$, if y_1 is odd and

$y_{i+1} = y_1 - ((x_1 + i + 1) \text{ MOD } 2)$, if y_1 is even.

for i=1..N-1